



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 6871

SERIAL NUMBER 10/824,857	FILING DATE 04/14/2004 RULE	CLASS 716	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 2102487-991181
-----------------------------	---------------------------------------	--------------	------------------------	--

APPLICANTS

Mutsunori Igarashi, Yokohama-shi, JAPAN;
 Takashi Mitsuhashi, Fujisawa-shi, JAPAN;

** CONTINUING DATA *****
 This application is a DIV of 10/122,402 04/12/2002 PAT 6,763,508

** FOREIGN APPLICATIONS *****
 JAPAN P2001-115780 04/13/2001

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
 ** 06/26/2004

Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance Verified and Acknowledged	STATE OR COUNTRY JAPAN SHEETS DRAWING 35 TOTAL CLAIMS 9 INDEPENDENT CLAIMS 2
Examiner's Signature: <i>[Signature]</i> Initials: <i>[Initials]</i>	

ADDRESS
 26379
 DLA PIPER RUDNICK GRAY CARY US, LLP
 2000 UNIVERSITY AVENUE
 E. PALO ALTO , CA
 94303-2248

TITLE
 Layout design system, layout design method and layout design program of semiconductor integrated circuit, and method of manufacturing the same

FILING FEE	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time)
------------	---	---